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09/939,602	08/28/2001	Takehiko Shimomura	027260-485	3292

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EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 04/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No. 09/939,602	Applicant(s) SHIMOMURA ET AL.	
	Examiner Dipakkumar Gandhi	Art Unit 2133	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 August 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3, 11/27/01.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: In figure 1, item 26 is not described in the specification. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Russell (US 5,404,358) in view of Tsukimori et al. (US 6,708,304 B1).

As per claim 1, Russell teaches a scan test system for a semiconductor device, comprising: a first semiconductor device including a first analog input/output pin existing on the analog input side thereof, a first internal circuit, and a scan register connected between said first input/output pin and said first internal circuit; a second semiconductor device including a second analog input/output pin on the analog input side thereof, a second internal circuit, and an analog wiring connecting said first analog input/output pin

and said second analog input/output pin (figure 1, col. 4, lines 32-60, col. 5, lines 23-26, col. 6, lines 6-9, Russell).

However Russell does not explicitly teach the specific use of a scan register connected between said second input/output pin and said second internal circuit.

Tsukimori et al. in an analogous art teaches a scan register connected between said second input/output pin and said second internal circuit (boundary scanning cells 40, semiconductor devices 81, 82, wiring board 80 in figure 19, Tsukimori et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Russell's patent with the teachings of Tsukimori et al. by including an additional step of using a scan register connected between said second input/output pin and said second internal circuit. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a scan register connected between said second input/output pin and said second internal circuit would provide the opportunity to conduct scan testing in the second internal circuit and inspect connections.

- As per claim 2, Russell and Tsukimori et al. teach the additional limitations.

Tsukimori et al. teach the scan test system for a semiconductor device, wherein at least one of the first and second semiconductor devices constitutes a register chain that serially connects a plurality of the scan registers within the device (figure 7 and 19, Tsukimori et al.).

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Russell (US 5,404,358) and Tsukimori et al. (US 6,708,304 B1) as applied to claim 2 above, and further in view of Blair et al. (US 5,428,624).

As per claim 3, Russell and Tsukimori et al. substantially teach the claimed invention described in claim 2 (as rejected above).

However Russell and Tsukimori et al. do not explicitly teach the specific use of the scan test system for a semiconductor device, wherein the scan register constituting the register chain complies with the JTAG specification, and constitutes a JTAG scan register, and the test system comprises control means for controlling this JTAG scan register.

Blair et al. in an analogous art teach that the building of devices to the JTAG specification requires that they have the ability to test themselves through built-in self test by allowing access to nodes and circuits which are otherwise physically inaccessible. This capability is based upon a test access port ("TAP") state machine, which allows control and access to a "boundary scan" architecture (col. 1, lines 47-55, Blair et al.). Blair et al. also teach that the JTAG boundary scan architecture has been utilized to detect existing faults (col. 1, lines 67-68, col. 2, line 1, Blair et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Russell's patent with the teachings of Blair et al. by including an additional step of using the scan test system for a semiconductor device, wherein the scan register constituting the register chain complies with the JTAG specification, and constitutes a JTAG scan register, and the test system comprises control means for controlling this JTAG scan register.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using JTAG scan register would provide the opportunity to test the circuit components through built-in self test by allowing access to nodes and circuits which are otherwise physically inaccessible.

6. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Russell (US 5,404,358) in view of Sturges (US 5,491,666) and Bloker et al. (US 5,768,196).

As per claim 4, Russell teaches a scan test system for a semiconductor device (col. 2, lines 53-57, Russell), comprising: said semiconductor device including: a first scan register connected between a digital/analog double function pin on the input side and an internal circuit (figure 1, col. 2, lines 58-67, col. 6, lines 9, lines 16-18, Russell).

However Russell does not explicitly teach the specific use of a second scan register connected between a digital input/output pin and said internal-circuit; a first register chain serially connecting a plurality of said first scan registers, each fetching the data input and outputting the result to the output side; a second register being connected to said first register chain and simultaneously serially connecting a plurality of said second scan registers, each fetching the data input and outputting the result to the output side.

Sturges in an analogous art teaches that the registers of the individual boundary scan circuits are joined to provide a series boundary scan register chain (col. 2, lines 60-62, Sturges). Sturges teaches that the test function of the boundary-scan circuitry is enabled by the TMS signals to allow data to flow to the TDO terminal. Thus, as may be seen, a serial path is provided through the boundary-scan circuitry of the circuit 22. Data may be transferred bit by bit through this serial path from the TDI terminal to the TDO terminal (col. 5, line 67, col. 6, lines 1-6, Sturges). Sturges teaches that FIG. 6 illustrates apparatus in accordance with the present invention. The figure illustrates an integrated circuit 22 including core logic which is separated into a plurality of individual portions only three portions 61, 62, and 63 of which are illustrated. Each of these portions has associated with it a controller 30 and a chain of boundary scan registers 26 (figure 6, col. 9, lines 32-38, Sturges).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Russell's patent with the teachings of Sturges by including an additional step of using a second scan register connected between a digital input/output pin and said internal-circuit; a first register chain serially connecting a plurality of said first scan registers, each fetching the data input and outputting the result to the output side; a second register being connected to said first register chain and simultaneously serially connecting a plurality of said second scan registers, each fetching the data input and outputting the result to the output side.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to rapidly test integrated circuitry and to allow separate portions of an integrated circuit to be individually tested utilizing boundary scan circuitry.

Russell also does not explicitly teach the specific use of a switching means bypassing at least one of said first and the second register chains and thereby connecting the data input to the output side.

Bloker et al. in an analogous art teach that as can be seen from FIG. 4, each shift register of circuit 36 is connected to two switching elements and a bypassing transistor such that the shift register can be switched off the chain without breaking up the shift register chain (figure 4, col. 4, lines 52-56, Bloker et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Russell's patent with the teachings of Bloker et al. by including an additional step of using a switching means bypassing at least one of said first and the second register chains and thereby connecting the data input to the output side.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a switching means bypassing at least one of said first and the second register chains and thereby connecting the data input to the output side would provide the opportunity to individually test separate portions of an integrated circuit utilizing boundary scan circuitry.

- As per claim 6, Russell, Sturges and Bloker et al. teach the additional limitations.

Bloker et al. teach a scan test system for a semiconductor device, wherein the switching means comprises: a first switch, a first bypass line that bypasses the first register chain, a second switch and a second bypass line that bypasses the second register chain, the first switch switches between the first register chain and the first bypass line, and the second switch switches between the second register chain and the second bypass line (figure 4, col. 4, lines 52-56, col. 6, lines 55-60, Bloker et al.).

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Russell (US 5,404,358), Sturges (US 5,491,666) and Bloker et al. (US 5,768,196) as applied to claim 4 above, and further in view of Blair et al. (US 5,428,624).

As per claim 5, Russell, Sturges and Bloker et al. substantially teach the claimed invention described in claim 4 (as rejected above).

However Russell, Sturges and Bloker et al. do not explicitly teach the specific use of a scan test system for a semiconductor device, wherein the scan register constituting the first and the second register chains complies with the JTAG specification, and constitutes a JTAG scan register, and the test system comprises control means for controlling this JTAG scan register.

Blair et al. in an analogous art teach that the building of devices to the JTAG specification requires that they have the ability to test themselves through built-in self test by allowing access to nodes and circuits which are otherwise physically inaccessible. This capability is based upon a test access port ("TAP") state

machine, which allows control and access to a “boundary scan” architecture (col. 1, lines 47-55, Blair et al.). Blair et al. also teach that the JTAG boundary scan architecture has been utilized to detect existing faults (col. 1, lines 67-68, col. 2, line 1, Blair et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Russell's patent with the teachings of Blair et al. by including an additional step of using a scan test system for a semiconductor device, wherein the scan register constituting the first and the second register chains complies with the JTAG specification, and constitutes a JTAG scan register, and the test system comprises control means for controlling this JTAG scan register.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using JTAG scan register would provide the opportunity to test the circuit components through built-in self test by allowing access to nodes and circuits which are otherwise physically inaccessible.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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